WHAT IS CLAIMED IS:

1. An integrated decision feedback equalizer and clock and data recovery circuit, comprising:

a decision feedback equalizer;

a clock recovery circuit; and

a flip-flop that comprises a portion of both the decision feedback equalizer and the clock recovery circuit.

2. The integrated decision feedback equalizer and clock and data recovery circuit of claim 1 wherein:

the decision feedback equalizer generates a binary data signal;

the clock recovery circuit generates an extracted clock signal;

the flip-flop is coupled to receive the binary data signal and the extracted clock signal to generate a flip-flop output signal; and

the flip-flop output signal is provided to the decision feedback equalizer to provide a first feedback signal and is provided to the clock recovery circuit to provide a first phase detector signal.

3. The integrated decision feedback equalizer and clock and data recovery circuit of claim 2 comprising a plurality of latches coupled to receive the flip-flop output signal to generate latch output signals, wherein the latch output signals comprise at least one second feedback signal for the decision feedback equalizer and second phase detector signals for the clock recovery circuit.

4. The integrated decision feedback equalizer and clock and data recovery circuit of claim 3 wherein the clock recovery circuit comprises an XOR circuit coupled to receive the binary data signal, the first phase detector signal and

the second phase detector signals to generate at least one phase detector output signal.

5. The integrated decision feedback equalizer and clock and data recovery circuit of claim 4 wherein the clock recovery circuit comprises a charge pump coupled to receive the at least one phase detector output signal.

6. The integrated decision feedback equalizer and clock and data recovery circuit of claim 5 wherein the clock recovery circuit comprises:

a loop filter coupled to receive an output signal from the charge pump; and

a voltage controlled oscillator coupled to receive an output signal from the loop filter to generate the extracted clock signal.

7. The integrated decision feedback equalizer and clock and data recovery circuit of claim 2 wherein the decision feedback equalizer comprises:

a multiplier coupled to receive the flip-flop output signal to generate a scaled feedback signal;

a summer coupled to receive an input data signal and the scaled feedback signal to generate a soft decision data signal; and

a slicer coupled to receive the soft decision data signal to generate the binary data signal.

8. The integrated decision feedback equalizer and clock and data recovery circuit of claim 3 wherein the decision feedback equalizer comprises:

a plurality of multipliers coupled to receive the flip-flop output signal and at least a portion of the latch output signals to generate scaled feedback signals;

a summer coupled to receive an input data signal and the

scaled feedback signals to generate a soft decision data signal; and

a slicer coupled to receive the soft decision data signal to generate the binary data signal.

9. The integrated decision feedback equalizer and clock and data recovery circuit of claim 2 wherein the flip-flop output signal comprises a recovered data signal.

10. The integrated decision feedback equalizer and clock and data recovery circuit of claim 3 wherein one of the latch output signals comprises a recovered data signal.

11. The integrated decision feedback equalizer and clock and data recovery circuit of claim 3 wherein:

the extracted clock signal clocks the flip-flop and the latches; and

at least two of the latches are clocked by different polarities of the extracted clock signal.

12. An integrated decision feedback equalizer and clock and data recovery circuit, comprising:

a summer coupled to receive an input data signal and at least one scaled feedback signal to generate a soft decision data signal;

a slicer coupled to receive the soft decision data signal to generate a binary data signal;

a flip-flop coupled to receive the binary data signal and an extracted clock signal to generate a first output signal;

a plurality of latches coupled to receive the first output signal to generate second output signals;

a charge pump coupled to receive at least one phase detector output signal associated with the first output signal and the second output signals;

a loop filter coupled to receive an output signal from

the charge pump;

a voltage controlled oscillator coupled to receive an output signal from the loop filter to generate the extracted clock signal; and

a multiplier coupled to receive the first output signal to generate the at least one scaled feedback signal.

13. The integrated decision feedback equalizer and clock and data recovery circuit of claim 12 comprising a plurality of XOR circuits coupled to receive the binary data signal, the first output signal and at least a portion of the second output signals to generate the at least one phase detector output signal.

14. The integrated decision feedback equalizer and clock and data recovery circuit of claim 12 comprising at least one multiplier coupled to receive at least a portion of the second output signals to generate the at least one scaled feedback signal.

15. The integrated decision feedback equalizer and clock and data recovery circuit of claim 12 wherein:

the extracted clock signal clocks the flip-flop and the latches; and

at least two of the latches are clocked by different polarities of the extracted clock signal.

16. An integrated decision feedback equalizer and clock and data recovery circuit, comprising:

a summer coupled to receive an input data signal and a plurality of scaled feedback signals to generate a soft decision data signal;

a slicer coupled to receive the soft decision data signal to generate a binary data signal;

a flip-flop coupled to receive the binary data signal and

an extracted clock signal to generate a first output signal;

a first latch coupled to receive the first output signal to generate a second output signal;

a second latch coupled to receive the second output signal to generate a third output signal;

an XOR circuit coupled to receive the binary data signal, the first output signal, the second output signal and the third output signal to generate at least one phase detector output signal;

a charge pump coupled to receive the at least one phase detector output signal;

a loop filter coupled to receive an output signal from the charge pump;

a voltage controlled oscillator coupled to receive an output signal from the loop filter to generate the extracted clock signal; and

a plurality of multipliers coupled to receive the first output signal and the third output signal to generate the scaled feedback signals.

17. The integrated decision feedback equalizer and clock and data recovery circuit of claim 16 wherein the third output signal comprises a recovered data signal.

18. The integrated decision feedback equalizer and clock and data recovery circuit of claim 16 wherein:

the extracted clock signal clocks the flip-flop, the first latch and the second latch; and

the first latch and the second latch are clocked by different polarities of the extracted clock signal.

19. The integrated decision feedback equalizer and clock and data recovery circuit of claim 16 comprising:

a third latch coupled to receive the third output signal to generate a fourth output signal; and

a fourth latch coupled to receive the fourth output signal to generate a fifth output signal;

wherein:

the multipliers are coupled to receive the fifth output signal to generate the scaled feedback signals; and

the XOR circuit is coupled to receive the fourth output signal to generate the at least one phase detector output signal.

20. The integrated decision feedback equalizer and clock and data recovery circuit of claim 19 wherein the fifth output signal comprises a recovered data signal.

21. The integrated decision feedback equalizer and clock and data recovery circuit of claim 19 wherein:

the extracted clock signal clocks the flip-flop, the first latch, the second latch, the third latch and the fourth latch;

the first latch and the second latch are clocked by different polarities of the extracted clock signal; and

the third latch and the fourth latch are clocked by different polarities of the extracted clock signal.

22. A method of recovering data from a received data signal, comprising:

summing a received data signal and at least one scaled feedback signal to generate a soft decision data signal;

digitizing the soft decision data signal to generate a binary data signal;

generating a first output signal by clocking the binary data signal into a flip-flop using an extracted clock signal;

generating a second output signal by clocking the first output signal into a first latch using the extracted clock signal;

generating a third output signal by clocking the second

output signal into a second latch using the extracted clock signal;

generating the at least one scaled feedback signal by multiplying the first output signal by a first equalization coefficient; and

generating the extracted clock signal according to the binary data signal, the first output signal, the second output signal and the third output signal.

23. The method of claim 22 wherein the first output signal comprises a recovered data signal.

24. The method of claim 22 comprising generating at least one input signal for a charge pump by XORing pairs of signals selected from the group consisting of the binary data signal, the first output signal, the second output signal and the third output signal.

25. The method of claim 22 wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal.

26. The method of claim 22 comprising generating the at least one scaled feedback signal by multiplying the third output signal by a second equalization coefficient.

27. The method of claim 26 wherein the third output signal comprises a recovered data signal.

28. The method of claim 26 comprising:

generating a fourth output signal by clocking the third output signal into a third latch using the extracted clock signal;

generating a fifth output signal by clocking the fourth output signal into a fourth latch using the extracted clock

signal;

generating the at least one scaled feedback signal by multiplying the fifth output signal by a third equalization coefficient; and

generating the extracted clock signal according to the fourth output signal.

29. The method of claim 28 wherein the fifth output signal comprises a recovered data signal.

30. The method of claim 28 comprising generating at least one phase detector output signal by performing XOR operations on the binary data signal, the first output signal, the second output signal, the third output signal and the fourth output signal.

31. The method of claim 28 wherein the third latch and the fourth latch are clocked by different polarities of the extracted clock signal.

32. The method of claim 28 wherein:

the flip-flop, the first latch and the third latch are clocked by the same polarity of the extracted clock signal, and

the second latch and the fourth latch are clocked by the same polarity of the extracted clock signal;

where the flip-flop, the first latch and the third latch are clocked by different polarities of the extracted clock signal than the second latch and the fourth latch.

33. An integrated retimer and phase detector, comprising:

a flip-flop comprising:

at least one data input for receiving a binary data signal generated from a received signal;

at least one clock input for receiving an extracted clock signal; and

at least one output for outputting a first output signal, wherein the first output signal comprises a feedback signal for a decision feedback equalizer and a first phase detector signal for a clock recovery circuit;

a first latch comprising:

at least one data input for receiving the first output signal;

at least one clock input for receiving the extracted clock signal; and

at least one output for providing a second phase detector signal for the clock recovery circuit; and

a second latch comprising:

at least one data input for receiving the second phase detector signal;

at least one clock input for receiving the extracted clock signal; and

at least one output for providing a second output signal, wherein the second output signal comprises a third phase detector signal for the clock recovery circuit.

34. The integrated retimer and phase detector of claim 33 wherein the second output signal comprises a second feedback signal for the decision feedback equalizer.

35. The integrated retimer and phase detector of claim 33 wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal.

36. The integrated retimer and phase detector of claim 33 comprising an XOR circuit coupled to receive the binary

data signal, the first phase detector signal, the second phase detector signal and the third phase detector signal to generate at least one phase detector output signal.

37. The integrated retimer and phase detector of claim 34 comprising:

a third latch comprising:

at least one data input for receiving the second output signal;

at least one clock input for receiving the extracted clock signal; and

at least one output for providing a fourth phase detector signal for the clock recovery circuit; and

a fourth latch comprising:

at least one data input for receiving the fourth phase detector signal;

at least one clock input for receiving the extracted clock signal; and

at least one output for providing a third feedback signal for the decision feedback equalizer.

38. The integrated retimer and phase detector of claim 37 wherein the third latch and the fourth latch are clocked by different polarities of the extracted clock signal.

39. The integrated retimer and phase detector of claim 37 comprising an XOR circuit coupled to receive the binary data signal, the first phase detector signal, the second phase detector signal, the third phase detector signal and the fourth phase detector signal to generate at least one phase detector output signal.

40. A method of retiming data and generating phase detector signals, comprising:

generating a first output signal by clocking a binary data signal into a flip-flop using an extracted clock signal;

providing the first output signal to a feedback loop of a decision feedback equalizer; and

generating at least one phase detector output signal using the first output signal.

41. The method of claim 40 comprising:

generating a second output signal by clocking the first output signal into a first latch using the extracted clock signal;

generating the at least one phase detector output signal using the second output signal;

generating a third output signal by clocking the second output signal into a second latch using the extracted clock signal;

providing the third output signal to the feedback loop of the decision feedback equalizer; and

generating the at least one phase detector signal using the third output signal.

42. The method of claim 41 wherein the first latch and the second latch are clocked by different polarities of the extracted clock signal.

43. The method of claim 41 wherein an XOR circuit is coupled to receive the binary data signal, the first output signal, the second output signal and the third output signal to generate the at least one phase detector output signal.

44. The method of claim 41 comprising:

generating a fourth output signal by clocking the third output signal into a third latch using the extracted clock signal;

generating the at least one phase detector output signal

using the fourth output signal;

generating a fifth output signal by clocking the fourth output signal into a fourth latch using the extracted clock signal; and

providing the fifth output signal to the feedback loop of the decision feedback equalizer.

45. The method of claim 44 wherein the third latch and the fourth latch are clocked by different polarities of the extracted clock signal.

46. The method of claim 44 wherein:

the flip-flop, the first latch and the third latch are clocked by the same polarity of the extracted clock signal, and

the second latch and the fourth latch are clocked by the same polarity of the extracted clock signal;

where the flip-flop, the first latch and the third latch are clocked by different polarities of the extracted clock signal than the second latch and the fourth latch.

47. The method of claim 44 wherein an XOR circuit is coupled to receive the binary data signal, the first output signal, the second output signal, the third output signal and the fourth output signal to generate the at least one phase detector output signal.